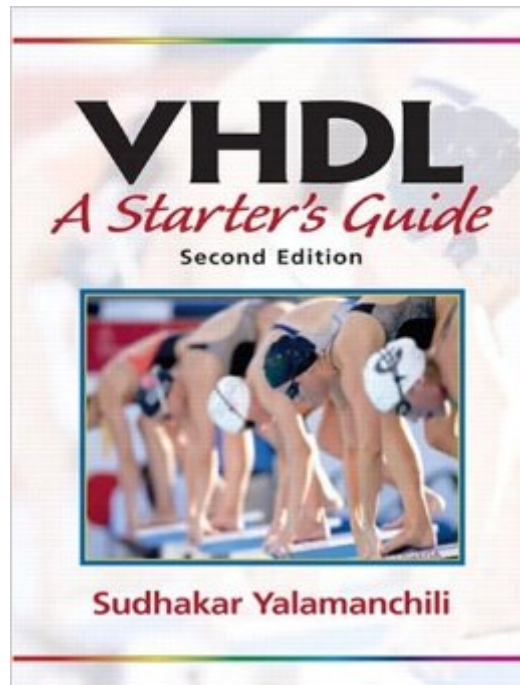The book was found

VHDL: A Starter's Guide (2nd Edition)

Synopsis

This handy reference gives readers a thorough grounding in the basic concepts and language of VHDL, and encourages them to apply what they have learned using realistic examples. Concepts are followed by examples and tutorials.   Adds appendices to support material: Includes a tutorial for a popular VHDL simulator; a handy reference to common VHDL packages; and a detailed template for a VHDL model illustrating the relative ordering of program constructs. Emphasizes development of readersâ ™ intuition and structured thinking about VHDL models without spending excessive time on advanced language features. Provides simulation and laboratory exercises that enable readers to quickly come up to speed in building useful, non-trivial models of digital systems. Provides tutorial descriptions and presentation of programming mechanics unique to CAD tools and environments. Includes examples, extensive use of timing diagrams, event lists and many tutorials for independent student study. Provides sample problems, many of which include worked solutions. Includes viewgraph masters and the VHDL source for all text examples. Â A useful reference for computer professionals who need to brush up on their VHDL knowledge.

Book Information

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Customer Reviews

This is a great book to teach yourself VHDL. I use this book along with the a microprocessor course that used Xilinx to teach myself VHDL. This book did wonders to get me started and familiar with the structure of VHDL. It also helped me get a new job in the industry of processor design. This book only uses the standard libraries: ieee.std_logic_1164.all, textio and standard

This book is exactly what it says it is: a VHDL Staters Guide. It is a great way to get started in VHDL, i'm finding this book clearly written, useful and interesting. This book has an emphisis on SIMULATION of VHDL, instead of SYTHESIS. This means that you don't need any silicon to start learning VHDL. However you will probably want another book on VHDL Systhesis as well, as you might want more in-depth information about sythesis. However this book is a great starting point, and clearly explains the syntax of VHDL and how to use it properly. VHDL is such a huge and powerful area that one 265 page book won't explain everything, but is a great way to begin!

I know there are many hardware design engineers and students who suffer from "VHDL anxiety" since it tends to seem alot less intuitive than verilog (especially in this age when C has surpassed ada as a common programming language taught at universities). For this reason Yalamanchili's VHDL Starter's Guide represents a nice contribution to the field. There is enough material in the guide to satisfy, say a senior computer-engineering student who is being intorduced for the first time.My only complaint about the book is its lack of appendices and specification of the entire language. So look somewhere else if this is the purpose for buying a VHDL book. However, as a place to start, it seems quite effective in developing the confidence needed to move on to the more technical aspects of synthesis and simulation.By the way, the author has written a thicker introductory hardcover book on VHDL published by Prentice Hall. The title is different, but it is virtually the same content. Little if anything was changed from that book to this starter guide. So be careful.

VHDL is a rather specialised programming language. It has subroutines, loops, if statements and other characteristics of general purpose procedural languages. But this book goes on to show that VHDL has very specific attributes that let you (hopefully easily) model circuits.These circuits might be combinatorial or sequential. For the latter, the book also goes into how this segues naturally into the idea of a finite state machine. A key concept in circuit design, and one that you need to master. To aid you, the book explains how you can build a behavioural model of a FSM. The theory of FSMs is not really expounded to any depth. An emphasis in this book is on using VHDL to model.You should note that VHDL is not an object oriented language. Though a minor aspect, that of being able to overload a subprogram name, seems to borrow from those languages.

It is a good introduction to the VHDL language and VHDL simulation. I was disapointed with the lack

synthesis discussion: how the different VHDL constructs can effect gate count and timing.

This is one of the best sources to start learning VHDL. The concepts are covered and explained well. Examples are excellent. Covers most of the features in a few pages. Figures need some improvement in terms of placement.

Mr Yalamanchili does a great job of introducing the reader to VHDL. The book is long enough to get you to understand the VHDL language, without being so long as to bore you to tears. After reading the book, I feel that I could design most any simple-medium complexity digital circuit in VHDL without much difficulty. My only complaint is the author's poor indenting of his code. This makes it difficult at times to follow the flow of his code. Other than this minor flaw, the book is perfect.

I have over 10 years of electronics design experience but have never used VHDL (CUPL and ABLE, yes). This book seems like it was written not by a hardware designer, but a by a programmer. Starting with zero knowledge of VHDL, his examples are hard to follow, and coding style is not consistant leading to confusion. I downladed a free tutorial program from Aldec.com and it has helped my understanding of the book GREATLY. In fact, it turns out the author references Aldec's Active-HDL simulator in appendix A.To Mr. Yalamanchili's credit, he does clearly state in his book, on page x of the preface, that this is supposed to be a supplementary text.I would recommend another book if you want to buy a "VHDL for Total Noobs" type that could also serve as a reference later on.Also, a glossary would have helped greatly.

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